Atty. Docket No. MP0299

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:	:
Pantas SUTARDJA et al.	: GROUP ART UNIT: 2611
APPLICATION NO: 10/634,218	:
FILED: AUGUST 4, 2003	: EXAMINER: WANG, Ted M.

FOR: ARCHITECTURES, CIRCUITS, SYSTEMS AND METHODS FOR REDUCING LATENCY IN DATA COMMUNICATIONS

I hereby certify that this document is being facsimile transmitted to the USPTO or deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 13, 2007

By: Jennie Heaton
Jennie Heaton

DECLARATION UNDER 37 C.F.R. 1.131

Mail Stop AMENDMENT
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

Now comes Hongying SHENG, who declares and states that:

1. I am a named inventor in the above-identified application.

2. I am currently employed by Marvell Semiconductor, Inc., as a Design Manager. My responsibilities include designing and developing circuitry for high-speed data communications and data storage products. I have been continuously employed by Marvell Semiconductor since September 1, 2000.

3. I received a Bachelor's degree in Electrical Engineering from Changchun Institute of Optical Devices and Physics in 1992.

4. I am familiar with the subject matter disclosed and claimed in the above-identified application.

5. I understand that claim 1 of the above-identified application is directed to an architecture for transferring data from a first device to a second device, comprising:

a) a clock recovery loop receiving said data from said first device, said clock recovery loop providing a recovered clock signal;

b) a filter circuit configured to filter information from said recovered clock signal and provide a transmitter clock adjustment signal that adjusts said transmitter clock in response to inputs from (i) said clock recovery loop and (ii) a transmitter clock circuit; and

c) a transmitter in communication with said filter circuit, configured to receive said transmitter clock adjustment signal and transmit said data to said second device in accordance with said transmitter clock signal.

6. The architecture defined in paragraph 5 above was conceived prior to April 23, 2003.

7. Attached hereto as Exhibit A is a copy of viewing screen printout from my workstation at Marvell of a design directory containing an integrated circuit design that includes an embodiment of the architecture defined in paragraph 5 above (hereinafter, the "working embodiment"). The file named "dpll.fm" contains a design that includes the working embodiment. The date of the design file is prior to April 24, 2003.

8. A specification defining the integrated circuit described in paragraph 7 and used internally at Marvell during product development was revised prior to April 24, 2003. An item identified in the change list of the revised specification relates to the working embodiment.

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9. The integrated circuit described in paragraph 7 and including the working embodiment was taped out at a wafer manufacturing fab prior to April 24, 2003.

10. Wafers containing the integrated circuit described in paragraph 7 (including the working embodiment) were manufactured after tape out. At least part of the manufacturing process occurred after April 24, 2003.

11. The manufactured integrated circuit was diligently tested after manufacturing. On information and belief, the testing of the manufactured integrated circuit did not reveal any operational defects in the architecture described in paragraph 5 above. From this result, I concluded that the working embodiment of the architecture defined in paragraph 5 above had actually been reduced to practice.

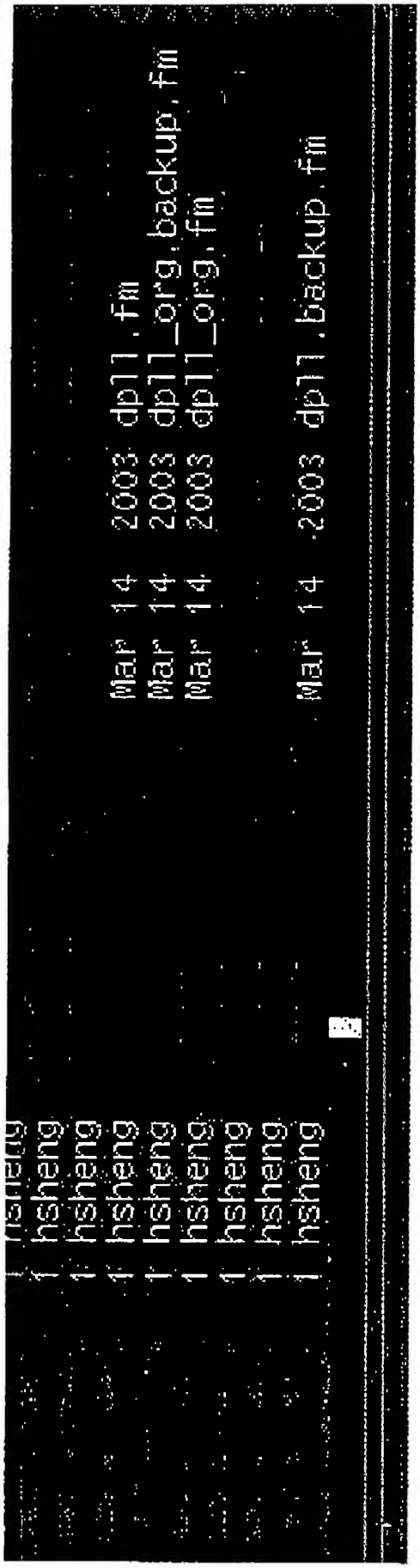
12. Further, Declarant sayeth not.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified application or any patent issued thereon or therefrom.

Hongying SHENG

07/12/2007
Date

EXHIBIT A



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